# Record-low 4 mΩ·mm$^2$ specific on-resistance for 20V Trench MOSFETs

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**Abstract – A process is shown by which both the specific on-resistance $R_{ds,on}$ and the gate-drain charge density $Q_{gd}$ can be reduced. Reduction of the $R_{ds,on}$ is achieved by optimising the channel profile (p-body) towards a more box-shaped profile. The $Q_{gd}$ is reduced by going to smaller trench dimensions below the I-line lithography limits, without using deep-UV lithography. For polygonal cell structures, it is shown that narrowing the trenches also gives further $R_{ds,on}$ reduction. Record values for $R_{ds,on}$ of 4 mΩ·mm$^2$ (at $V_{gs}$ = 10V) have been obtained for a 20V Trench MOSFET with a 2 µm cell pitch. Furthermore, for a 'conventional' 30V Trench MOSFET, we obtained an $R_{ds,on}$ of 7 mΩ·mm$^2$ (at $V_{gs}$ = 10V) by a more box-shaped p-body profile.**

## I. INTRODUCTION

For Trench MOSFETs used in Voltage Regulator Modules, the conduction and switching power losses in these transistors should be reduced. For a SyncFET this implies reduction of the specific on-resistance $R_{ds,on}$ and for a ControlFET reduction of the $R_{ds,on}$ and the gate-drain charge density $Q_{gd}$. The Figure-Of-Merit: FOM=$R_{ds,on}$·$Q_{gd}$ is generally used in order to describe the switching performance of the ControlFET. For low voltage devices, the channel resistance is the most significant contribution to the $R_{ds,on}$. One way to reduce the channel resistance is by optimising the channel (or p-body) doping profile [1]. However, to our knowledge no extensive experimental investigation of this has been reported in literature so far. In [1] it was found that the optimum p-body profile was a box-shaped one. Additionally, reducing the channel resistance can be achieved by going to smaller cell pitches [2] and, for polygonal cell pitches narrowing the gate-trench width. The latter also reduces the switching losses since these are determined by the gate-drain charge density $Q_{gd}$.
In this work a process is presented in which both the $R_{ds,on}$ and $Q_{gd}$ can be reduced by approximating a box-shaped channel profile as much as possible and by narrowing the gate-trenches. The aim was to narrow the trenches below the limits of I-line lithography, without using deep-UV lithography.

## II. OPTIMISING CHANNEL PROFILE

The unified mobility model [3] was used to analytically compare different channel profiles. In Figure 1 two different channel profiles are shown used for comparison. The first is an actual SIMS profile of a Trench MOSFET, the second an analytical box-shaped profile with the same top doping concentration and channel dose. A comparison of their channel resistance as a function of gate-source voltage is shown in figure 2.

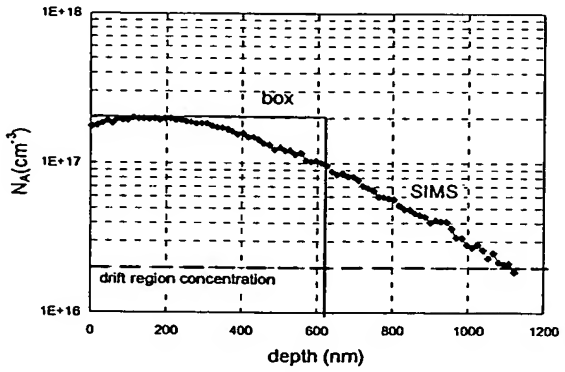


Figure 1: Channel profiles used to illustrate the influence of the profile on the channel resistance.

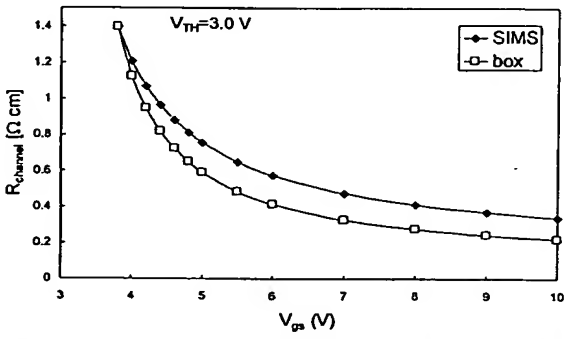


Figure 2: Analytical channel resistance as a function of gate voltage $V_{gs}$ for the different profiles shown in Figure 1. One can clearly see the effect of decreased channel resistance for the box-shaped profile at higher gate voltages. At low $V_{gs}$ the resistance is similar, due to the same p-body dose.

At gate-source voltages in excess of ~ 5 V the channel resistance of the box-shaped profile is almost 40% lower. This is caused by the fact that at relatively large electric fields the mobility is limited by interface scattering [4], causing the channel length to be dominant in determining the channel resistance. At lower gate-source voltages the mobility is limited by impurity scattering [5]. Therefore, at $V_{gs} < 5$ V, the channel resistance of both profiles is comparable. This example shows that for obtaining lower specific on-resistances the channel length should be as small as possible. To create a box-shaped profile, the single p-body implant was replaced with multiple implants and the thermal budget that these implants experienced was minimised. This was realised by performing the implants after the high thermal budget of the gate oxidation.

Two different profiles were investigated, named p-body A and B with depths of 0.7 µm and 0.8 µm respectively. Both Boron p-body profiles, together with the Arsenic source profile and the Phosphorous drift EPI, are shown in figure 3.

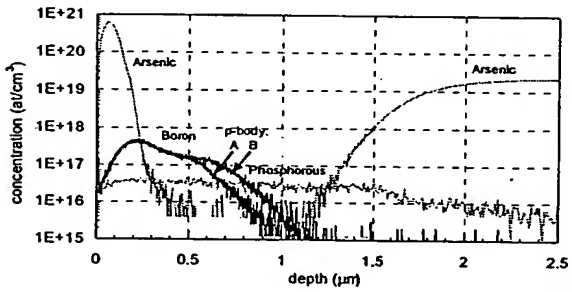


Figure 3: SIMS data of the doping profiles of the Trench MOSFET. Two different p-body profiles have been implanted: A and B.

## III. TRENCH FORMATION

For a constant cell pitch, the $Q_{gd}$ can be reduced by going to narrower trenches. For polygonal cell structures (e.g. a square cell structure), this also reduces the $R_{ds,on}$ since the channel density increases. To go below the optical limits of I-line lithography, inside spacers have been used to create smaller trench dimensions (Figure 4). The process starts with an oxide hard mask opening (0.7 µm for 2 µm cell pitch) after which a relatively thin nitride layer (e.g. 10 nm) and a TEOS layer are deposited. The thickness of the TEOS layer defines the desired trench width after spacer etch. The nitride layer is the etch stop layer for this spacer etch. After spacer etch, the nitride stop layer is removed and trenches are etched down to the desired depth. In this process the pitch size has been varied from 2 µm to 7 µm. In figure 5 a SEM cross-section of a 2 µm pitch device is shown with a trench width of 370 nm. The narrowest trenches that have been obtained are 300 nm wide.

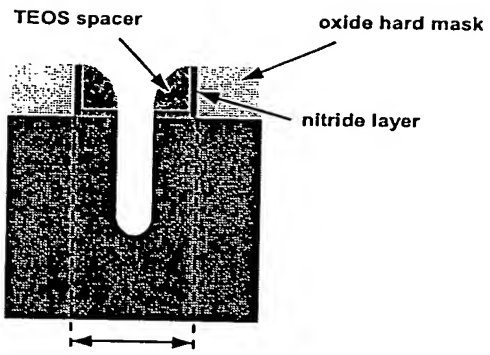


Figure 4: Cross-section of a narrow trench created with a standard I-line lithography oxide hard mask opening and inside spacers.

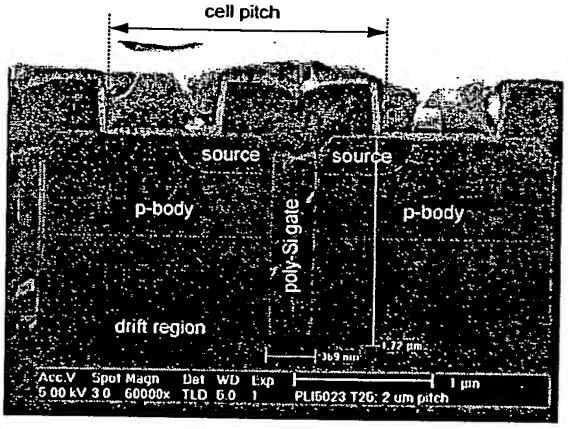


Figure 5: SEM cross-section of a Trench MOSFET with narrow trenches.

## IV. MEASUREMENTS

On-wafer measurements show that for square-shaped cell structures $R_{ds,on}$ reduces when the trench width decreases (Figure 6) as mentioned in section III. As a comparison, no significant trench width dependence of the $R_{ds,on}$ has been observed for stripe-shaped cell structures (2 µm pitch). This can be explained by the fact that for a stripe-shaped cell structure, narrowing the trenches does not increase the channel density of the device. Figure 7 shows the on-wafer measured drain-source current $I_{ds}$ as a function of the gate-source voltage $V_{gs}$ for both p-body profiles A and B, on logarithmic and linear scale. These characteristics have been obtained from 2 µm pitch devices with a square-shaped cell structure, a trench depth of 1.5 µm and a trench width of 300 nm. For both devices a threshold voltage $V_T$ of around 2.3V has been found and a relatively low leakage current in the subthreshold region can be seen.

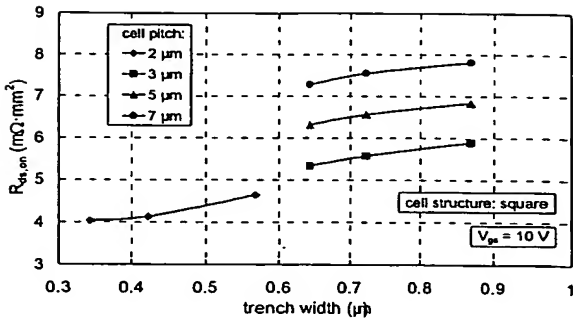


Figure 6: Measured specific on-resistance $R_{ds,on}$ as a function of the trench width for different square-shaped cell pitches. The trench depth is 1 µm and the channel profile is p-body A. The estimated substrate resistance is 1.4 mΩ·mm².

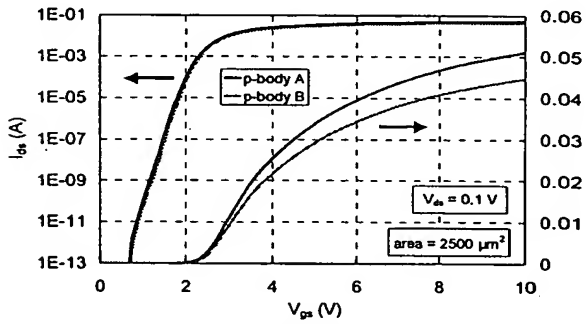


Figure 7: Measured drain-source current $I_{ds}$ as a function of the gate-source voltage $V_{gs}$ for both p-body profiles A and B ($V_{ds}$ = 0.1 V). The measured devices have a square-shaped cell structure with a pitch of 2 µm, a trench depth of 1.5 µm and a trench width of 300 nm.

The on-state characteristics in figure 8 show a increase of the drain-source current $I_{ds}$ at around $V_{ds}$ = 4V. This increase is attributed to the parasitic source/p-body/drift bipolar transistor that is switched on due to the hole current generated by avalanche near the trench bottom. Experiments to investigate this are on-going.

A typical off-state drain-source breakdown curve is plotted in figure 9. The source-drain breakdown $BV_{ds}$ is found at 21V. This result is obtained for a 2 µm pitch devices with a square-shaped cell structure, 1 µm deep and 570 nm wide trenches and p-body A. It turned out that for such an aggressive profile like p-body A (0.7 µm) in combination with 4e16 $cm^{-3}$ drift-EPI, no punch through effects are present.

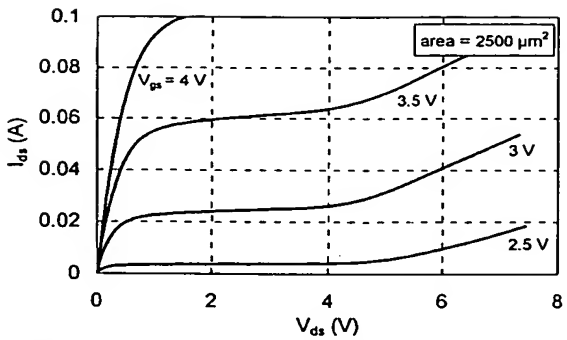


Figure 8: Measured drain-source current $I_{ds}$ as a function of the drain-source voltage for different gate-source voltages $V_{gs}$. The device has a square cell geometry with a pitch of 2 µm, a trench depth of 1 µm, a trench width of 570 nm and p-body B. We assume that the sudden increase of the current at $V_{ds}$ = 4V is due to avalanche.

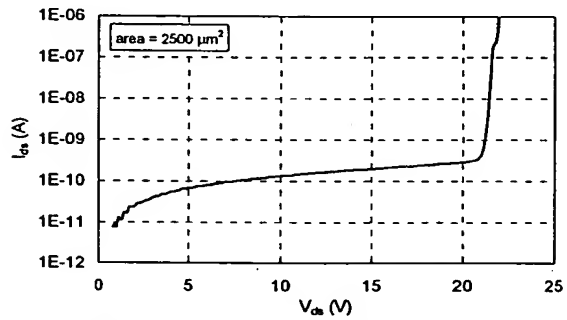


Figure 9: Measured off-state drain-source current $I_{ds}$ as a function of the drain-source voltage $V_{ds}$ with an avalanche breakdown at 21 volts. The device has a square-shaped cell structure with a pitch of 2 µm, a trench depth of 1 µm, a trench width of 570 nm and p-body A.

The best result that we obtained for $R_{ds,on}$ is 4 mΩ·mm² (at $V_{gs}$ = 10V) in combination with a source-drain breakdown $BV_{ds}$ of 21V. These values are measured on devices with a 2 µm stripe-shaped cell pitch, p-body A and trenches of 1.5 µm deep and 300 nm wide. Because of the relatively deep trenches compared with the p-body depth, these devices have a relatively high $Q_{gd}$ and therefore a high FOM of 69 mΩ·nC. The best result for $R_{ds,on}$ in combination with the FOM is 5 mΩ·mm² and 18 mΩ·nC respectively, at $V_{gs}$ = 10V ($BV_{ds}$ = 21V). These values have been obtained from on-wafer measured devices with a 2 µm stripe-shaped cell pitch, p-body B and trenches of 1 µm deep and 400 nm wide. Our results show that a more optimised (box-shaped) p-body profile already gives relatively low values of $R_{ds,on}$. This can also be seen from a 'conventional' 30V Trench MOSFET that have been made, which gives an $R_{ds,on}$ of 7 mΩ·mm² at $V_{gs}$ = 10V. This device has a 2 µm stripe-shaped cell pitch and contains trenches of 1.3 um deep and 700 nm wide. The p-body profile is p-body A. The best FOM we obtained for such a 30V Trench

MOSFET, is 30 mΩ·nC ($R_{ds,on}$ = 7.5 mΩ·mm² at $V_{gs}$ = 10V). This device has a 2 µm stripe-shaped cell pitch and contains trenches of 1 µm deep and 700 nm wide. The p-body profile is p-body A.

The best results from our work compared with early published values [6,7,8], are shown in figures 10 and 11. Note that in [6] and [7] cell pitches of 1-1.1 µm are reported, in contrast with our work in which the smallest cell pitch is 2 µm.

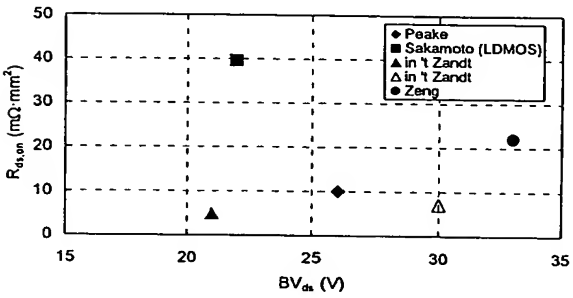


Figure 10: Values of $R_{ds,on}$ as a function of drain-source breakdown voltage $BV_{ds}$ from this work compared with earlier published values [6,7,8]. The closed triangle is a value measured from a 21V Trench MOSFET with a 2 µm stripe-shaped cell pitch, p-body A, and trenches of 1.5 µm deep and 300 nm wide. The open triangle is a value measured from a 30V Trench MOSFET with a 2 µm stripe-shaped cell pitch, p-body A, and trenches of 1.3 µm deep and 700 nm wide.

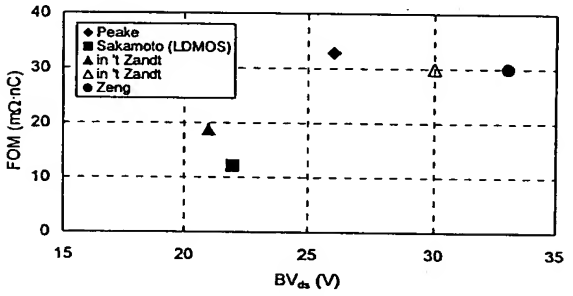


Figure 11: Values of FOM as a function of drain-source breakdown voltage $BV_{ds}$ from this work compared with earlier published values [6,7,8]. The closed triangle is a value measured from a 21V Trench MOSFET with a 2 µm stripe-shaped cell pitch, p-body B, and trenches of 1 µm deep and 400 nm wide. The open triangle is a value measured from a 30V Trench MOSFET with a 2 µm stripe-shaped cell pitch, p-body A, and trenches of 1 µm deep and 700 nm wide.

## V. CONCLUSIONS

It was shown that by optimising the p-body profile towards a more box-shaped profile, the $R_{ds,on}$ of Trench MOSFETs is reduced. In order to create a more box-shaped p-body profile, the use of multiple implants turned out to be very effective. For a given cell pitch, the $Q_{gd}$ reduces when the trench width decreases. The use of inside spacers makes it possible to reduce the trench width without going into deep-UV lithography. For polygonal cell pitches, narrowing the trenches gives even a further reduction of the $R_{ds,on}$. Record values of $R_{ds,on}$ = 4 mΩ·mm² (at $V_{gs}$ = 10V) for a 20V Trench MOSFET, and $R_{ds,on}$ = 7 mΩ·mm² (at $V_{gs}$ = 10V) for a 30V Trench MOSFET have been obtained. These results have been obtained with 2 µm pitch devices with stripe-shaped cell structures.

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